AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated below. The language being added is underlined ("__") and the language being deleted contains either a strikethrough ("——") or is enclosed by double brackets ("[[ ]]").

Listing of Claims

1. (Currently Amended) An apparatus for forming a sequence of N-byte second words from bytes forming a sequence of N-byte first words, where N is any integer greater than 1, the apparatus comprising:

a main memory for storing a plurality of bytes, each at a separate address;

a cache memory for storing a plurality of bytes, each at a separate address, wherein [[and]] the size of the main memory is larger than that of the cache memory; and

a control circuit, coupled to the main memory and the cache memory, for comparing the size of the cache memory with a product of the data length, N and a desired interleaving/de-interleaving depth, D to produce a control signal, for writing bytes of each first word into either the main memory or the cache memory according to the control signal, for reading bytes out of the cache memory or the main memory and forming each second word ~~there from~~ according to the control signal such that each second word comprises the bytes of more than one of the first words.

2. (Original) The apparatus in accordance with claim 1 wherein the cache memory and the control circuit are implemented within a single integrated circuit (IC), and wherein the main memory is external to the IC.

3. (Original) The apparatus in accordance with claim 1 wherein

the control circuit operates in a burst read mode in which it reads bytes stored at a plurality of sequential addresses of the main memory whenever it read accesses the main memory,

wherein the control circuit operates in a burst write mode in which it writes bytes to a plurality of sequential addresses of the main memory whenever it write accesses the main memory, and

wherein the control circuit independently read and write accesses each individual address of the cache memory whenever it reads a byte from or writes a byte to the cache memory.

4. (Original) The apparatus in accordance with claim 1

wherein the control circuit writes bytes of each first word into the main memory so that they are addressed in the main memory in an order in which those bytes appear in the first word,

wherein the control circuit reads bytes out of the main memory and writes them to the cache memory, and

wherein the memory control circuit forms each second word from bytes it reads out of the cache memory.

5. (Original) The apparatus in accordance with claim 1

wherein the control circuit writes bytes of each first word into the cache memory,

wherein the control circuit reads bytes of the first words out of the cache memory and writes them to the main memory such that they are addressed in the main memory in an order in which they are to appear in the second words, and

wherein the control circuit forms each second word from bytes it reads out of the cache memory and the main memory.

6. (Original) The apparatus in accordance with claim 4 further comprising:

an input buffer for receiving and storing bytes forming each first word, wherein the control circuit reads bytes forming each first word from the input buffer and writes them to the main memory so that they are addressed in the main memory in

an order in which the bytes appear in that first word, and also reads bytes forming first words out of the input buffer and writes them to the cache memory, and

an output buffer, wherein the control circuit forms the second words in the output buffer by reading bytes out of the cache memory and writing them into the output buffer.

7. (Original) The apparatus in accordance with claim 5 further comprising:

an input buffer for receiving and storing each first word, wherein the control circuit transfers bytes forming each first word from the input buffer to the cache memory; and

an output buffer, wherein the control circuit forms the second words in the output buffer by reading bytes out of the main memory and out of the cache memory and writing them into the output buffer.

8. (Original) The apparatus in accordance with claim 6 wherein the control circuit writes every byte of each first word into the main memory.

9. (Original) The apparatus in accordance with claim 6 wherein the control circuit writes some, but less than all, bytes of each first word into the main memory.

10. (Original) The apparatus in accordance with claim 7 wherein the control circuit writes every byte of each first word into the main memory.

11. (Original) The apparatus in accordance with claim 7 wherein the control circuit writes every byte of each first word into the main memory.

12. (Currently Amended) A method for forming a sequence of N-byte second words from bytes forming a sequence of N-byte first words, wherein N is any integer greater than 1, the method comprising the steps of:

comparing the size of the cache memory with a product of the data length, N and a desired interleaving/de-interleaving depth, D to produce a control signal,

writing bytes of each first word into a main memory or into a cache memory according to the control signal,

transferring bytes between the main memory and the cache memory according to the control signal, and

reading bytes of the cache memory or the main memory and forming each second word according to the control signal ~~from them~~ such that each second word comprises the bytes of more than one of the first words.

13. (Original) The method in accordance with claim 12

wherein a plurality of bytes are read from a plurality of sequential addresses of the main memory in a burst read mode of accessing the main memory whenever the main memory is read accessed,

wherein a plurality of bytes are written to a plurality of sequential addresses of the main memory in a burst write mode whenever the main memory is write accessed, and

wherein a single address of the cache memory is independently read or write accessed whenever the cache memory is read or write accessed.

14. (Currently Amended) The method in accordance with claim 12

wherein the step of writing comprises writing bytes of each first word into the main memory so that they are addressed in the main memory in an order in which those bytes appear in that first word, and

wherein the step of transferring comprises reading bytes out of the main memory and writing them to the cache memory, and wherein the step of reading comprises forming each second word from bytes read out of the cache memory.

15. (Original) The method in accordance with claim 12

wherein the step of writing comprises writing bytes of each first word into the cache memory, wherein the step of transferring comprises reading bytes out of the cache memory and writing them to the main memory, and

wherein the step of reading comprises forming each second word from bytes read out of the cache memory and the main memory.

16. (Currently Amended) The method in accordance with claim 12

wherein the step of writing comprises, for each first word, the substeps of:

storing bytes forming each first word in an input buffer,

reading bytes of each first word stored in the input buffer and writing them to the main memory, and

reading selected bytes of each first word stored in the input buffer and writing them to selected addresses of the cache memory;

wherein the step of transferring comprises reading bytes out of the main memory and writing them into the cache memory; and

wherein the step of writing comprises reading bytes forming the second word out of the cache memory and writing them into an output buffer.

17. (Currently Amended) The method in accordance with claim 12

wherein the step of writing comprises, for each first word, the substeps of:

storing bytes forming the first word in an input buffer, and

reading bytes of the first word from the input buffer and writing them to the cache memory,

wherein the step of transferring comprises reading bytes forming the first word out of the cache memory and writing them to the main memory, and

wherein the step of writing comprises, for each second word, the substeps of

reading bytes forming the second word out of the main memory and out of the cache memory; and

writing them into an output buffer to form the second word in the output buffer.

18. (Original) The method in accordance with claim 16 wherein the substep of reading bytes of the step of writing comprises reading all bytes of the first word out of the input buffer and writing them into the main memory.

19. (Original) The method in accordance with claim 16 wherein the substep of reading bytes of the step of writing comprises reading less than all bytes of the first word out of the input buffer and writing them to the main memory.

20. (Original) The method in accordance with claim 17 wherein the step of transferring comprises reading all bytes of the first word written into the cache memory back out of the cache memory and writing them to the main memory.

21. (Original) The method in accordance with claim 17 wherein the step of transferring comprises reading less than all of the bytes of the first word written into the cache memory back out of the cache memory and writing them into the output buffer.

22. (Previously Canceled)

23. (Previously Presented) The apparatus of claim 1, wherein the size of the cache memory is not smaller than a product of a maximum of the interleaving/de-interleaving depth and a number of bytes read from or written to a sequential address of the main memory during each read or write access.

24. (Previously Presented) The apparatus of claim 23, wherein the size of the main memory is not smaller than a product of a largest allowable interleaving/de-interleaving depth and a largest allowable byte width of code word.

25. (Previously Presented) The method of claim 12, wherein the size of the cache memory is not smaller than a product of a maximum of the interleaving/de-interleaving depth and a number of bytes read from or written to a sequential address of the main memory during each read or write access.

26. (Previously Presented) The method of claim 25, wherein the size of the main memory is not smaller than a product of a largest allowable interleaving/de-interleaving depth and a largest allowable byte width of code word.